What is claimed is:

1. A die-level opto-electronic device, comprising:

a semiconductor die having edges and a photonic device exposed on a first surface;

a conductive structure formed in the die and away from the edges of the die, the conductive structure being exposed on a second surface of the die that opposes the first surface, wherein the conductive structure is electrically connected to the photonic device; and

an optically transparent laminate attached to the first surface so as to overlay the photonic device.

2. The die-level opto-electronic device of claim 1 wherein the photonic device is an image sensor.

3. The die-level opto-electronic device of claim 1 further comprising an under bump metallization pad attached to the second surface, the under bump metallization pad being electrically connected to the conductive structure.

4. The die-level opto-electronic device of claim 3 wherein the under bump metallization pad is redistributed so as to occupy a different location on the second surface than the conductive structure.

5. The die-level opto-electronic device of claim 1 further comprising a solder bump deposited on the conductive structure so as to extend beyond the second surface.

6. The die-level opto-electronic device of claim 1 wherein the optically transparent laminate comprises a glass.

7. A semiconductor wafer, comprising:

a substrate having a plurality of photonic devices exposed on a first surface;

a plurality of conductive structures formed in the substrate, the plurality of structures being exposed on a second surface of the substrate that opposes the first surface, wherein ones of the plurality of structures are electrically connected to associated ones of the plurality of photonic devices; and

an optically transparent laminate attached to the first surface so as to overlay the plurality of photonic devices.

8. The semiconductor wafer of claim 7 wherein the plurality of photonic devices further comprises a plurality of image sensors.

9. The semiconductor wafer of claim 7 further comprising a plurality of under bump metallization pads attached to the second surface, ones of the plurality of under bump metallization pads being electrically connected to associated ones of the plurality of conductive structures.

10. The semiconductor wafer of claim 9 wherein the plurality of under bump metallization pads is redistributed so as to occupy different locations on the second surface than the plurality of conductive structures.

11. The semiconductor wafer of claim 7 further comprising a plurality of solder bumps, wherein ones of the plurality of solder bumps are deposited on associated ones of the plurality of conductive structures so as to extend beyond the second surface.

12. The semiconductor wafer of claim 7 wherein the optically transparent laminate comprises a glass.

13. A method of fabricating an opto-electronic device, comprising:

creating a hole in the first surface of a semiconductor die;

depositing a conductive material within the hole;

electrically coupling the conductive material to a photonic device located on said first surface;

processing a second surface of the semiconductor die so as to expose the conductive material on said second surface, wherein the second surface opposes the first surface; and

attaching an optically transparent laminate on the first surface so as to overlay the photonic device.

14. The method of claim 13 further comprising placing an under bump metallization pad proximate to the second surface, wherein the under bump metallization pad is electrically connected to the conductive material.

15. The method of claim 14 wherein said placing further includes redistributing the under bump metallization pad at a different location on the second surface than the conductive material.

16. The method of claim 13 further comprising placing a solder bump proximate to the conductive material and extending beyond the second surface.

17. The method of claim 13 wherein said processing includes etching the second surface of the die so as to expose the conductive material.

18. The method of claim 13 wherein said processing includes etching the second surface of the die so as to expose the conductive material.

19. The method of claim 13 wherein said creating includes etching the hole in the first surface of the die.

20. The method of claim 13 wherein said creating includes drilling the hole in the first surface of the die.